AN OUTPUT-CAPACITOR-LESS LOW DROPOUT (LDO) VOLTAGE REGULATOR WITH SUPERIOR TRANSIENT RESPONSE

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ABSTRACT:
In this paper, an output-capacitor-less Low Dropout (LDO) Voltage Regulator implemented in a standard 0.13-µm CMOS process is introduced. The proposed scheme makes use of Bulk Modulation Technique for improving the performance of low-drop-out (LDO) voltage regulators. Improvements in load driving capability and recovery time when the technique is applied to a conventional LDO regulator are confirmed. The proposed LDO regulator has ~1.5% load regulation and is able to delivers up to 5 mA of load current while providing 1 V drawing 99.0 µA from a 1.2 V supply. It has been observed that the proposed circuit offers better stability as well as improvement in the load current delivery and recovery time of 0.16 µs for no-load to full-load and full-load to no-load transitions.

KEYWORDS—*Bulk modulation technique, capacitor-less LDO, power supply rejection, low-drop-out voltage regulator, low-power, recovery time.*

I. INTRODUCTION

Low Dropout (LDO) voltage regulators can be operated with a very small input-output voltage differential and these are commonly used in electronic systems particularly in portable or low-power applications. Their main function is to provide a stable supply voltage by nullifying the noises and ripples caused by imperfect power sources and/or variable load currents. They are ideal to be embedded in system-on-chip (SOC) solutions due to their relatively simple structure and few external components [1], [3].

The LDO regulator determines the overall performance of the internal power supply. For portable applications, power efficiency is a critical requirement to prolong battery cycle. Therefore, low quiescent current and dropout voltage are essential. Several techniques are proposed to improve the transient responses without increasing the quiescent current [2].Recovery time of the regulator and its power consumption are among the important design considerations in portable devices and many biomedical implants. The linear voltage regulator topology shown in Fig.1 typically consists of a pass element, an error amplifier and a resistive feed-back network. Using PMOS transistor as pass element may introduce stability issues and thus typically requires a large external capacitor [10]. To improve this issue particularly in fully integrated designs, capacitor-less monolithic regulators have been proposed [1], [4], [14].

Recently, a lot of researchers have proposed various strategies to produce output capacitor-less LDO regulators [10]–[12] and to improve the recovery time, as well as load and line regulation performance of integrated LDOs [1], [5]–[10]. Meanwhile, output capacitor-free LDOs can greatly reduce the area of the printed circuit board by removing large off-chip output capacitors. Hence, output capacitor-free LDOs are widely used in handheld products powered by Li battery due to their low-noise characteristics and few external components [11], [12]. Many of the capacitor-less LDOs are based on pole-splitting compensation approach [10], [12].In many of such designs the improvement in recovery

time is achieved by employing additional and often fairly complex circuitry [10], [12] which in turn results in higher power consumption and/or larger chip area.

In this brief, a fast transient response capacitor-less LDO regulator using an alternative simple technique that modulates the bulk voltage of the pass element to enhance the performance of the LDO is presented. The concept of the proposed LDO regulator and circuit implementation are discussed in Section II. Experimental results are given in Sections III. Finally, the conclusion of this brief is given in Section IV.

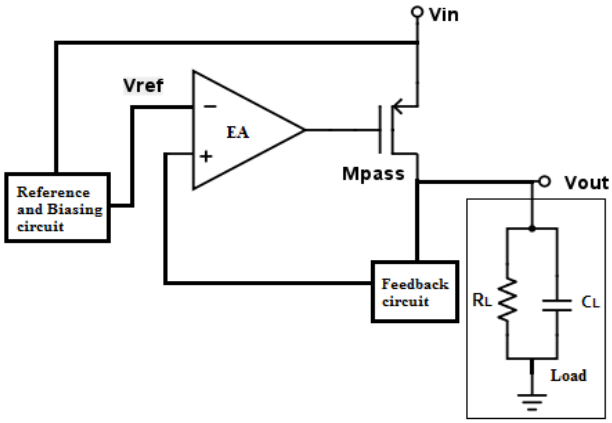

Fig.1. LDO Voltage Regulator

II. THE PROPOSED LDO STRUCTURE WITH BULK MODULATION TECHNIQUE

The change of threshold voltage of a MOS transistor as a function of its source to bulk voltage is referred to as "body effect" and the proposed technique takes advantage of body effect to reduce the threshold voltage of the pass transistor for any given current load. For long-channel devices, the threshold voltage can be approximated by [8]:

$$|V_{th}| = |V_{th0}| + \gamma\left(\sqrt{V_{SB} + 2|\emptyset_F|} - \sqrt{2|\emptyset_F|}\right) \quad (1)$$

where V_{th} is the threshold voltage of the device for $V_{SB} \neq 0$, and V_{th0} is the nominal threshold voltage value for $V_{SB} = 0$, γ is the body-bias coefficient and $2|\emptyset_F|$ is the surface potential.

For PMOS transistors $\gamma < 0$, from (1), by decreasing the bulk voltage in PMOS transistors the absolute value of the threshold voltage decreases. For a fixed V_{SG}, this change in the threshold voltage will result in an increase in the drain-source current and vice versa. The body effect is sometimes referred to as "back-gate effect" since the effect of the bulk voltage on the drain-source current is same as that of the gate voltage, [8].

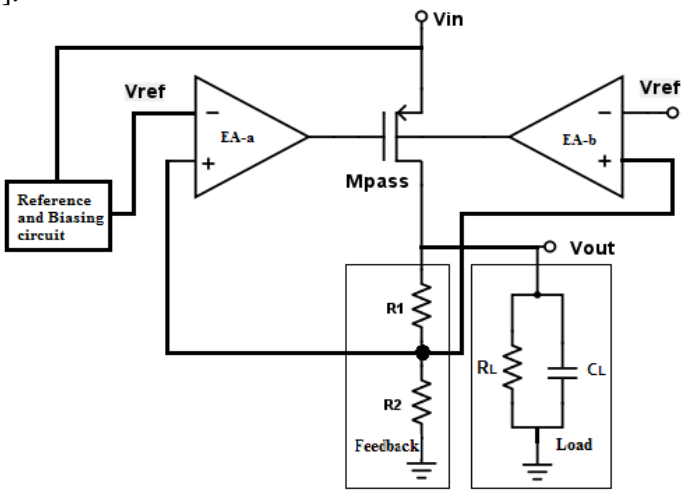

Fig.2. Block diagram of proposed LDO Voltage Regulator

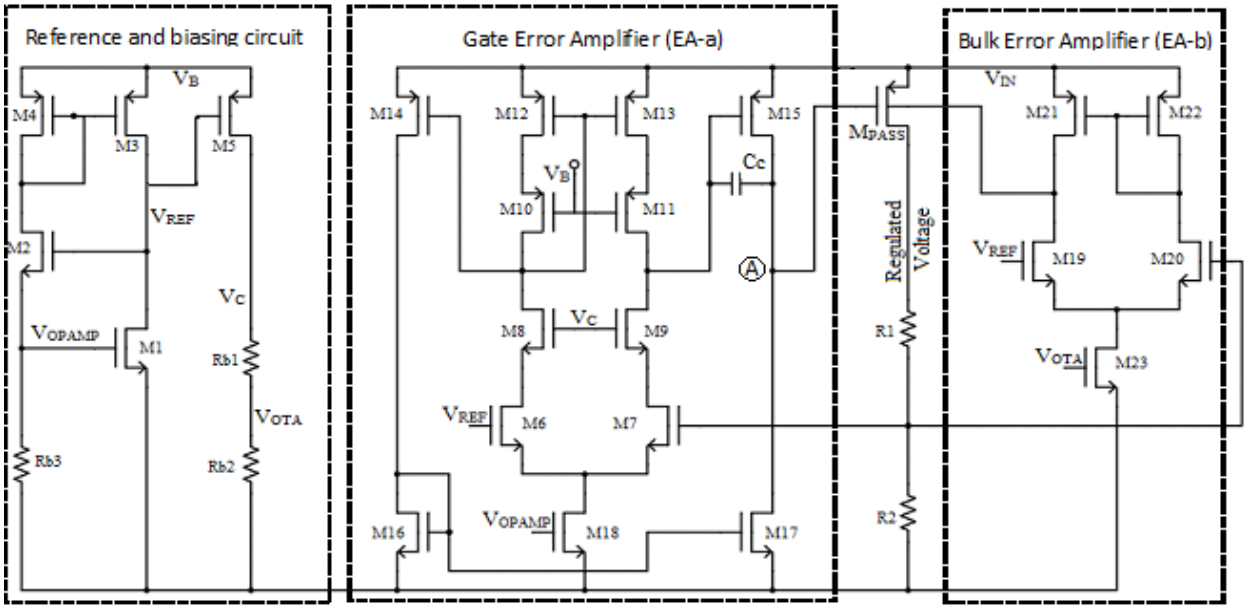

Fig.3. Schematic of proposed LDO Voltage Regulator

In the proposed structure Fig.2, bulk of the pass transistor is connected to the output of an extra error amplifier with a higher bandwidth (i.e. EA-b) and amplifier with a larger DC gain (i.e. EA-a) is connected to the gate of the pass transistor. Therefore, the main error amplifier will provide the high DC gain for accurate regulation while the bulk amplifier provides agile response to the output changes and higher overall bandwidth. The overall schematic of the presented LDO regulator is illustrated in Fig.3. Maximum load current which is decided by the size of the pass transistor is also improved.

Note that in the proposed technique, special attention must be paid to the design to make sure the bulk-source diode of the pass transistor does not turn on, that is the bulk voltage of the pass transistor should not go below 1.2 V minus one diode forward voltage. The prototype is implemented in a 0.13-μm CMOS technology.

The improvements resulted from the proposed technique by applying it to a conventional LDO regulator are demonstrated, however, one can apply the proposed technique to other LDO architectures as well.

Different attributes of the proposed bulk modulation technique –

A. Driving Capability

The main benefits of modulating the bulk of the pass transistor is that for a given aspect ratio of the pass transistor, bulk modulation improves the output current delivery i.e. one can achieve the same current delivery with a smaller pass transistor using bulk modulation technique [10]. By reducing the threshold voltage of the pass transistor by applying bulk voltage which is lower than the source voltage i.e. V_{IN} of the regulator we can improve the current delivery of the LDO. Note that we are interested to set the DC voltage level of the pass transistor bulk as low as possible to maximize the driving capability of the pass transistor.

B. Transient Behavior

When the load current suddenly drops in a conventional amplifier, the output of EA-a will increase up to V_{IN} to reduce the pass transistor current to regulate the output voltage. In the proposed technique, when bulk modulation is applied to the pass transistor, the "faster" error amplifier (EA-b) will sense the change and increases the bulk voltage of the pass transistor from its equilibrium voltage up to the maximum value of V_{IN}. At equilibrium, the inputs of both error amplifiers are equals to the reference voltage. This will cause an increase of the threshold voltage of the pass transistor which further helps to reduce the current of the pass transistor and thus shortens the recovery time. In the proposed regulator, using bulk modulation of the pass transistor, the bandwidth of the overall system is increased [11], [18]. Furthermore, by using the second error amplifier (i.e., EA-b) the overall slew

time of the output node, namely, I_{slew}, is decreased. Thus, as depicted in Fig. 4, both recovery time and the output voltage change are decreased. Note that by applying the proposed bulk modulation technique, one can use a smaller aspect ratio pass transistor while achieving the same current delivery of the conventional regulator. The smaller pass transistor implies a smaller parasitic capacitance and thus a faster operation. In addition, since the bulk amplifier (EA-b) is designed to have a higher bandwidth than the standard error amplifier (EA-a), it can sense the changes in the output voltage faster, and thus result in a faster operation and less voltage fluctuations.

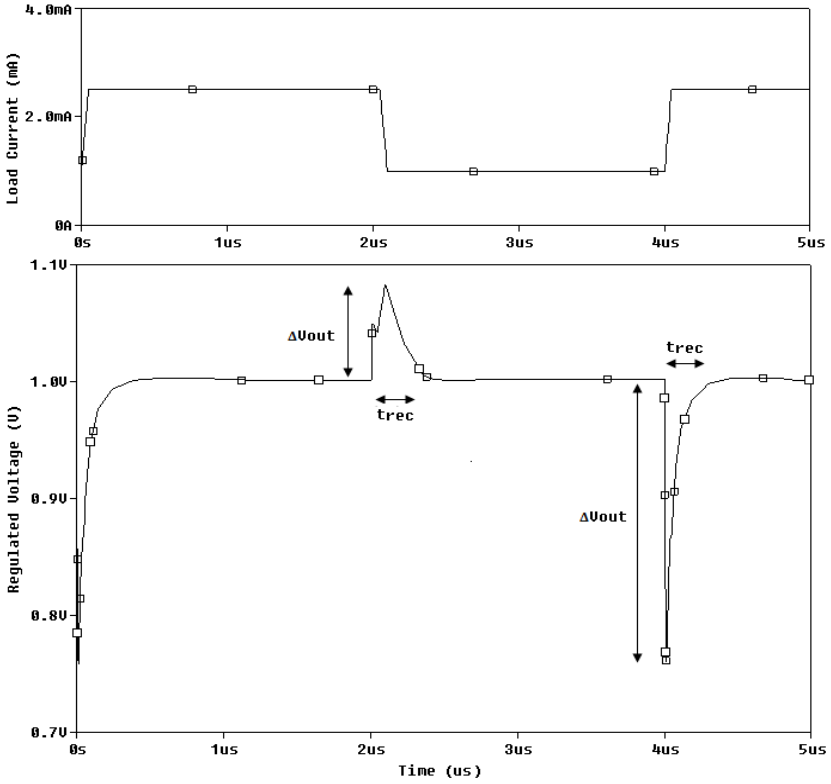

Fig. 4. Recovery time analysis for LDO regulator in sudden decrease and increase of the load current.

C. Stability Analysis

The low-frequency small-signal open-loop gain of the proposed regulator can be written as

$$A_V = \beta_f \cdot R_{out} \cdot \left[\left(A_{1-dc} \cdot g_m^{pass}\right) + \left(A_{2-dc} \cdot g_{mb}^{pass}\right)\right] \quad (2)$$

where$\beta_f$is the feedback gain and is equal to R_2 / R_1 + R_2, R_{out} = $R_L \| r_{ds}^{pass} \cong R_L$ is the open-loop output resistance of the regulator, where r_{ds}^{pass} is the small-signal drain-source output resistance of the pass transistor, R_L is the equivalent resistance of the load which is typically much smaller than r_{ds}^{pass}, A_{1-dc} and $A_{2-dc}$are the low-frequency small-signal voltage gain of the main and bulk error amplifiers, respectively, and g_m^{pass} and $g_{mb}^{pass}$are the small-signal gate and back-gate (body) trans-conductance of the pass transistor. From (equation 2), the above open-loop gain equation we can surmise that the overall open-loop gain of the regulator is a function of the sum of the gains of the two error amplifiers. It can be shown that the open-loop phase response of the regulator at any given frequency would follow the phase of the error amplifier that has a higher gain at that frequency. Referring to the open-loop gain and the phase response of the regulator shown in Fig. 5, the open-loop structure has a dominant pole which belongs to *EA-a* (namely, the dominant pole of the op-amp in *EA-a*, ω_{opamp}). This pole is at node A shown in Fig. 3 and is independent of the load current of the regulator.

$$\omega_{opamp} = \frac{1}{\left(C_{gate} + C_c + C_{opamp}\right) \cdot r_{opamp}} \quad (3)$$

where, C_{gate} is the total parasitic capacitance seen at the gate of the pass transistor,$C_{opamp} = C_{par}^{n} + C_{par}^{p}$is the parasitic capacitance seen at the output stage of the *EA-a* and r_{opamp} is the small-signal output resistance of the *EA-a*.

The second pole is the dominant pole of the *EA-b* which is given by:

$$\omega_{OTA} = \frac{1}{(C_{bulk} + C_{ota}) \cdot r_{ota}} \tag{4}$$

where, C_{bulk} is the total parasitic capacitance seen at the bulk of the pass transistor, $C_{ota} = C_{par}^{n} + C_{par}^{p}$is the parasitic capacitance seen at the output stage of the *EA-b* and r_{ota} is the small-signal output resistance of the *EA-b*. Note that C_{par}^{p} and C_{par}^{n} are the total parasitic capacitance at the output node of the *EA-a* and *EA-b* amplifiers, that are introduced by NMOS and PMOS transistors connected to that node respectively. A zero is created in between these two poles due to the use of the two amplifiers in parallel. To further study the reason of having this zero and its frequency, consider two amplifiers $A_1 = G_1\big(1 / 1 + (s / p_1)\big)$ and $A_2 = G_2\big(1 / 1 + (s / p_2)\big)$ and $A_3 = A_1 + A_2$ (from equation 2) where G_1 and G_2 are DC gain, p_1, p_2 are amplifiers' poles. In practice, as it is also the case in the proposed LDO $G_2 \times p_2 \gg G_1 \times p_1$ and $G_1 \gg G_2$ and $p_2 \gg p_1$. The parallel combination of the two amplifiers (or linear systems) has the following transfer function:

$$A_3 = (G_1 + G_2)\frac{1 + \frac{s}{z_1}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{5}$$

where $z_1 = p_1 p_2 (G_1 + G_2) / (p_1 G_1 + p_2 G_2)$. By simplifying (5) using the above mentioned assumptions, we have:

$$A_3 \cong G_1 \frac{1 + \frac{s}{\widetilde{z_1}}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{6}$$

where$\widetilde{z_1} = p_1 G_1 / G_2$. The introduced zero, $\widetilde{z_1}$ is located at the frequency where the gain of the two systems are equal. In our case, this zero is at the frequency ω_z where $A_1(\omega_z) \cdot g_m^{pass} = A_2(\omega_z) \cdot g_{mb}^{pass}$. Note that, in general, A_3 benefits from both high DC gain and high bandwidth characteristics. Since this zero is always in between the above mentioned poles, it compensates the phase drop caused by the first dominant pole. The third pole of the system is located at the output node of the regulator and is usually at a higher frequency (compared to the above mentioned two poles) and is given by:

$$\omega_L = \frac{1}{\big(C_L + C_{par}\big) \cdot R_{out}} \tag{7}$$

where, $C_L$and C_{par} are the load and parasitic capacitance at the output node of the regulator. The variation of the load current which can be interpreted as the variation of R_L may cause an instability in the system. The problem arises when the value of the load current is very small and at the same time large capacitive load is attached to the system. In this case ω_L will be at lower frequencies and may fall below the unity gain frequency (UGF) of the regulator, and therefore may deteriorate the phase margin.

In a conventional LDO regulator, any decrease in the output load current will lead to an increase in the open-loop voltage gain of the regulator (refer to equation 2), and consequently, it will increase the UGF of the conventional regulator as given by UGF $\cong \omega_{opamp} \cdot$ Av. This increase in UGF may jeopardize the phase margin and therefore the stability of the overall system. Note that over the frequency range where the open-loop voltage gain is greater than 1 (0 dB) the closed-loop system will provide regulation irrespective of whether the pass transistor is operating in saturation or linear region.

In the proposed regulator, the frequency of the second dominant pole of the regulator depends on the load current. When the load current decreases the gain of the regulator will increase but at the same time C_{bulk} will increase as well. This increase of C_{bulk} is a consequence of the change in the pass transistor operating point. Since a part of the parasitic capacitance seen from the bulk of the transistor

is the parasitic capacitance between bulk and drain, due to the increase in the bulk drain voltage gain the Miller equivalent capacitance seen at the bulk will increase. The increase of C_{bulk} consequently leads to a decrease of the frequency of ω_{OTA} as a second dominant pole of the regulator. Since the effect of the first dominant pole (ω_{opamp}) has been compensated by ω_z, the unity gain frequency in the proposed regulator is more robust to changes of the load current. As a result, the proposed regulator retains a positive phase margin over a wider output capacitance range.

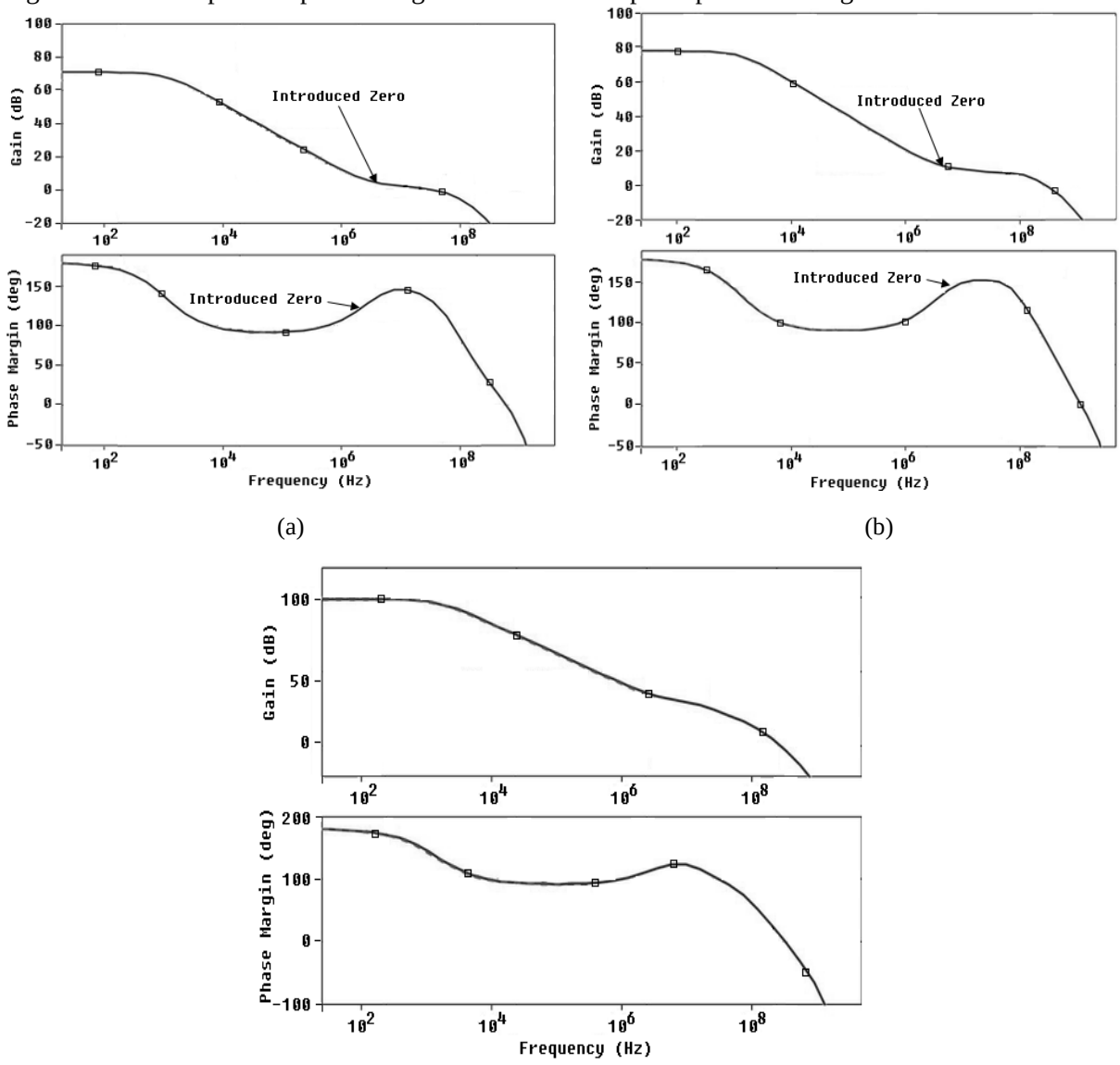

Fig. 5. Simulated open-loop bode diagram of the proposed LDO configuration with and without bulk modulation technique for load currents of (a) 3 mA, (b) 2 mA, and (c) 0 mA (no-load).

III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed circuit is fabricated in a 0.13 µm CMOS technology and the steady-state (DC), transient, and frequency response of the regulator is obtained using Cadence (OrCAD capture, Pspice) tools.

A. DC Response

Fig. 6 presents the total quiescent current of the proposed regulator for different temperatures at I_{Load} = 3mA. As we expected the regulator with the bulk modulated technique will drain more current in higher temperature since we have addition error amplifier. The proposed regulator draws 99.04 µA

from a 1.2 V supply for I_{Load} = 3mA, which is 53% more than the conventional regulator due to the use of additional bulk amplifier. In particular, EA-a draws 38.6 µA, EA-b draws 51.01 µA, and reference voltage and biasing circuits draw 9.43 µA from the supply. Fig. 7 illustrates the DC line regulation of the proposed regulator and it confirms that using the proposed bulk modulator technique the regulator works with a lower supply voltage. This feature can be attributed to the fact that the threshold voltage of the pass transistor at low input voltages is decreased which in turn makes the regulator more responsive to lower input voltages. The lower turn-on voltage can be very useful in low-power applications. The magnitude of the measured DC line regulation for the proposed regulator is 1.48%. To obtain the DC response of the regulator, input voltage V_{IN} is applied in the form of ramp.

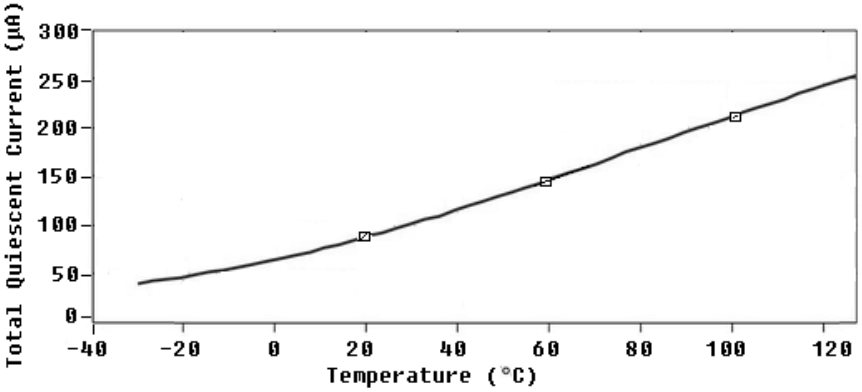

Fig. 6. Total quiescent current versus temperature at I_{Load} = 3mA

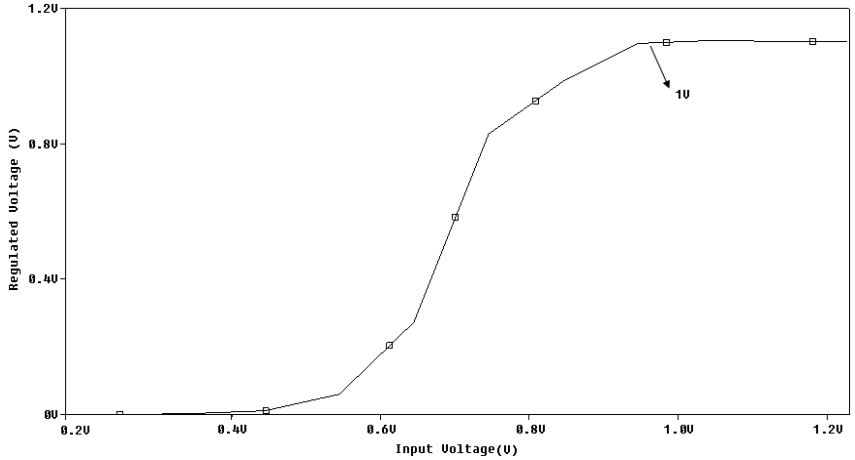

Fig. 7. DC response of the proposed regulator to different input DC voltage.

B. Transient Response

Start-up time is one of the important performance metrics for any LDO regulator which indicates how fast the regulator can provide the regulated voltage. Fig. 8 presents the startup time of the proposed regulator. In this experiment a pulse input voltage with raising time of 5 ns is applied to the regulator at 2 mA of load current. Note that the proposed bulk modulation technique has an improved start-up of 0.32µs. This improvement can be attributed to the wideband bulk error amplifier as well as the lowering of the threshold voltage of the pass transistor.

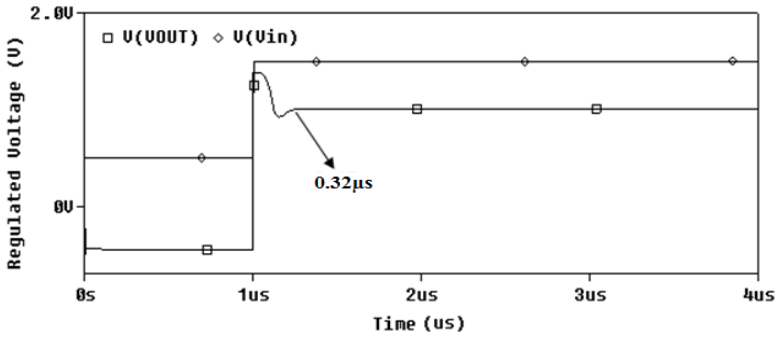

Fig. 8. Measured start-up transition of the regulators for current load of 2 mA.

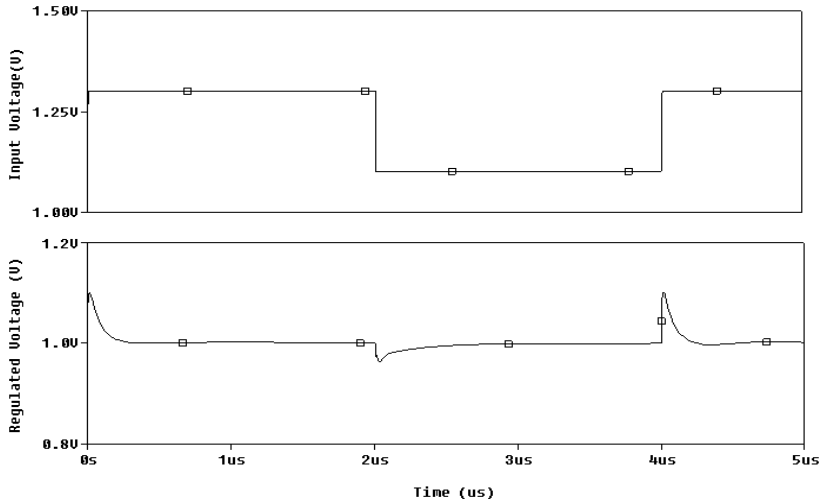

Fig. 9. Line regulation for load current of 2 mA.

Line regulation is another important performance parameter of LDOs. The measured line regulation performance is presented in Fig. 9 and it is observed that the proposed technique slightly enhances the line regulation performance.

C. Frequency Response

Simulation results shown in Fig. 5 validates the overall voltage gain obtained in open-loop gain equation (equation 2) and verify the position of the zero. Fig. 10 illustrates the effect of the parallel EA-b on power supply rejection (PSR) of the regulator. As expected, the improvement in the line regulation is achieved by adding the extra bulk error amplifier, EA-b. To further investigate the line regulation performance of the proposed circuit at different frequencies, a PSR measurement is conducted. And it is confirmed that the PSR of the proposed bulk-modulated regulator is slightly better than the conventional regulator. As shown in Table I the proposed regulator achieves superior PSR. However, this PSR performance can be attributed to the following reasons. The main reason is the relatively small full load current of the proposed regulator as compared to the similar designs which in turn facilitates larger loop-gain and thus better power supply rejection ratio. Secondly, the wide bandwidth error amplifier EA-b offers a better PSR at higher frequencies.

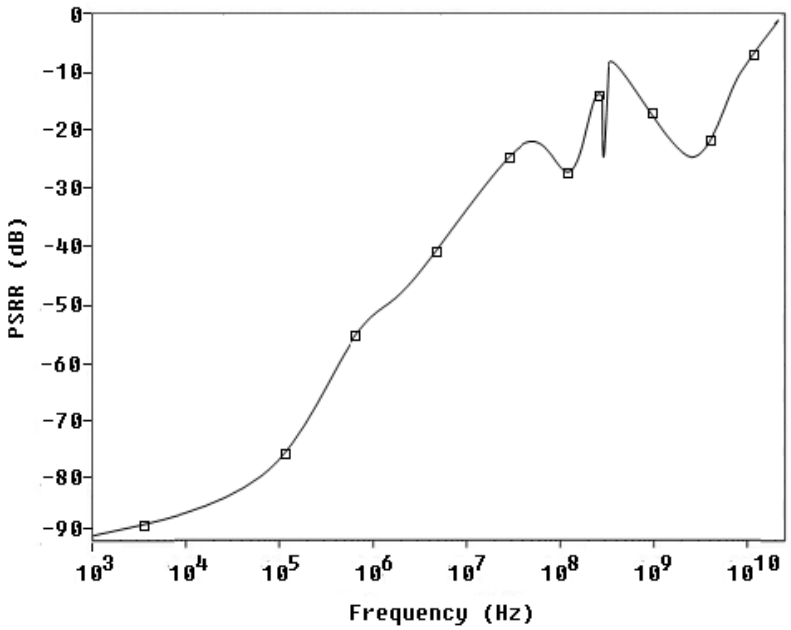

Fig. 10. Measured and post-layout simulated PSR performance of regulators while supplying 1 mA of load current.

Table 1: Performance Summary And Comparison

	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[7]	This work w/o BM	This work with BM
Year	2010	2010	2010	2011	2012	2013	2013	2014	2015	2015
Technology (µm)	0.09	0.18	0.13	0.13	0.18	0.18	0.065	0.18	0.13	0.13
V_{in} (V)	1	1.2-2.5	1.2	0.9	1.6	1.4-1.8	1.2	1.8	1.2	1.2
V_{out}(V)	0.85	0.9-1.8	1	0.8	1-1.2	1.2	1	1.6	1	1
V_{DO} (mV)	150	541	200	100	400-600	200-600	200	200	200	200
$I_Q^{max\text{-}load}$ (µA)	33-145	35	45	1.33	120	40	0.9	55	44.03	99.04
Area normalized to 0.00245 mm^2	5.075	126.53	10.20	12.42	65.3	17.95	6.94	57.14	~1	1
Settling time (µs)	N/A	100	0.07	28	4.8	1.172	6	< 6	1.43	0.16
Full load: $I_{Load\text{-}max}$ (mA)	140	150	2	50	5	100	100	50	3	5
Load Regulation (mV/mA)	0.043	0.101	< 0.5	N/A	0.122	N/A	0.3	0.14	0.023	0.015
PSR (dB)	-56 @ 10MHz, -30 @ 30MHz	-64.3 @ 1kHz	-55 @ 1Mz	N/A	-65 @ 1kHz	N/A	-58 @ 10kHz	-70@ 1MHz, -37@ 10MHz	-93 @ 1kHz -58.23 @ 1MHz -41.15@10MHz	-93.6@1kHz -57.11@1MHz -36.15@10MHz
Closed-loop bandwidth	N/A	20 kHz	100 kHz	80-200 kHz	680 kHz	10 MHz	N/A	N/A	27 MHz	117 MHz
∆Vout (mV)	94	196	120	~250	0.61	100	69	120	50	50

IV. CONCLUSION

The proposed technique modulates the bulk voltage of the pass element to enhance the performance of the LDO. The extra error amplifier used to drive the bulk of the pass transistor draws an additional 51 µA current while on average it improves the load delivery capability by 79% and achieves the recovery time of 0.16 µs i.e. more than 10 times improvement. It improves line and load regulations as well as the driving capability of the regulator while it reduces the power consumption of the LDO as compared to conventional LDOs with similar performance. Furthermore, as compared to conventional approaches, the technique increases the closed-loop bandwidth of the regulator which in turn improves the transition recovery time for no-load to and from full-load conditions, thus, making it suitable for applications where load conditions may change rapidly. The technique is particularly suited for low-power applications such as biomedical implants and portable devices. Table I presents the performance summary of the proposed LDO and compares it with a conventional LDO regulator without bulk modulation as well as other state-of-the-art LDOs. The proposed Bulk Modulation technique can also be applied to other LDO structures.

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